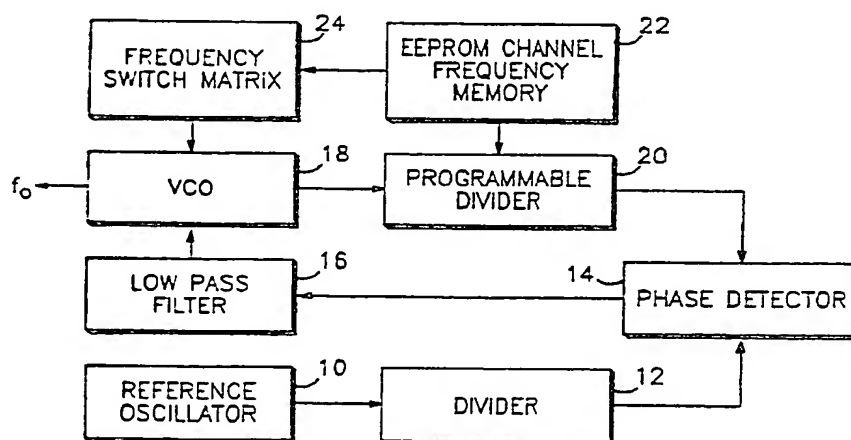




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ : H03B 19/00, H03L 7/00	A1	(11) International Publication Number: WO 89/ 06456 (43) International Publication Date: 13 July 1989 (13.07.89)
<p>(21) International Application Number: PCT/US88/04547</p> <p>(22) International Filing Date: 19 December 1988 (19.12.88)</p> <p>(31) Priority Application Number: 141,380</p> <p>(32) Priority Date: 7 January 1988 (07.01.88)</p> <p>(33) Priority Country: US</p> <p>(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).</p> <p>(72) Inventor: DAVIS, Walter, Lee ; 10948 N.W. 3rd Street, Coral Springs, FL 33065 (US).</p> <p>(74) Agents: PARMELT E. Steven, G. et al.; Motorola, Inc., Intellectual Property Department, 1303 East Algonquin Road, Schaumburg, IL 60196 (US).</p>	<p>(81) Designated States: AT (European patent), AU, BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).</p> <p>Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>	

(54) Title: **LOW VOLTAGE AND LOW POWER FREQUENCY SYNTHESIZER**

(57) Abstract

A low power and low voltage frequency synthesizer includes a memory (22) containing information to provide divisor information to the variable divider (20) of a phase locked loop and information to select predetermined values of capacitance to connect to the frequency determining resonant network of the VCO (18) to provide a coarse tuning. This tuning is then further modified by the normal operation of the phase locked loop.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	ML	Mali
AU	Australia	GA	Gabon	MR	Mauritania
BB	Barbados	GB	United Kingdom	MW	Malawi
BE	Belgium	HU	Hungary	NL	Netherlands
BG	Bulgaria	IT	Italy	NO	Norway
BJ	Benin	JP	Japan	RO	Romania
BR	Brazil	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	LI	Liechtenstein	SN	Senegal
CH	Switzerland	LK	Sri Lanka	SU	Soviet Union
CM	Cameroon	LU	Luxembourg	TD	Chad
DE	Germany, Federal Republic of	MC	Monaco	TG	Togo
DK	Denmark	MG	Madagascar	US	United States of America
FI	Finland				

-1-

LOW VOLTAGE AND LOW POWER FREQUENCY SYNTHESIZERFIELD OF THE INVENTION

The field of the invention relates to frequency synthesizers for use in communication devices and more particularly, to frequency synthesizers which operate on very low voltages and reduced power.

BACKGROUND OF THE INVENTION

5 Frequency synthesizer phase locked loops have been utilized in communication transceivers for some period of time. The normal approach is to use a varactor tuned voltage controlled oscillator in combination with controlled modulus frequency
10 divisors in the phase locked loop to produce the desired output frequency. In these prior art techniques, a varactor, or voltage controlled capacitor, is commonly used to vary the resonant frequency of the VCO tuning network in accordance
15 with a control voltage. This approach requires the use of high varactor control voltages, typically, 12 volts or more, to achieve the VCO tuning range that is needed for feedback transceiver applications. In the case of small portable devices, especially
20 single cell receivers, the voltage required and power consumed by this varactor tuning approach in a frequency synthesizer would consume excessive power and would result in a very shortened battery life.

25 The present invention is intended to overcome this disadvantage of the prior art by providing a channel frequency memory which provides not only the

-2-

appropriate phase locked loop divisors for a PLL-VCO synthesizer but also alters the VCO frequency tuning network by selectively adding discrete capacitors to the frequency determining network of the VCO as a
5 course frequency adjustment. Thus, only a low voltage, low varactor network with a much reduced tuning range is required to fine tune the VCO and allow the loop to operate properly.

SUMMARY OF THE INVENTION

10 It is an object of the invention to provide a low voltage, low powered frequency synthesizer which is capable of operating on at most a two cell battery.

15 It is a further object of the invention to provide a very low power frequency synthesizer utilizing a VCO that is tuned by a combination of additive capacitors and a low voltage varactor network to cover a broad range of frequencies.

20 It is yet a further object of the invention to provide a phase locked loop frequency synthesizer which does not require multi-cell batteries in conjunction with voltage multipliers to achieve reasonable tuning ranges.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a frequency synthesizer in employing the present invention.

25 FIG. 2 is an additional detailed block diagram of a portion of the frequency synthesizer shown in FIG. 1.

-3-

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows a phase locked loop frequency synthesizer, which includes many parts common with the frequency synthesizers of the prior art, but also includes additional devices as taught by the present invention. Reference oscillator 10 provides a fixed frequency reference signal to a divider 12. The divided down frequency from divider 12 is provided as a first input to phase detector 14 which provides a signal through a low pass filter 16 as a first input of VCO 18. One output of VCO 18 is connected through a programmable divider 20 and back to a second input to phase detector 14. A memory 22, for the preferred embodiment, an electrically erasable programmable read only memory containing channel frequency divisor information, modifies programmable divider 20 to adjust the division ratio of the two signals incoming to phase detector 14 so that the VCO produces an output of F_0 that is appropriate for the desired frequency synthesizer output. The operation of the elements as presently described, is well known in the art as a normal phase locked loop frequency synthesizer.

Channel frequency memory 22 not only includes division information supplied to the programmable divider 20 to adjust the output frequency, but it further includes information supplied to a frequency switch matrix 24 which adds discrete capacitors directly into the frequency determining resonant network of VCO 18. Thus, instead of requiring the high voltages and high current drains that are needed to drive the voltage controlled reactive elements used in prior art VCO tuning networks, fixed capacitance values can be selectively added to the frequency determining resonant network to

-4-

provide the appropriate range of frequency outputs that are necessary to provide a broadband frequency synthesis. This is achieved while conserving the normal power that would be required to achieve that tuning.

FIG. 2 shows, in a more detailed manner, the structure of frequency matrix 24. The channel frequency data corresponding to the desired frequency and divisor information which is supplied to divider 20 from EEPROM memory 22 is supplied to a frequency to capacitance decoding logic block 26. This frequency to capacitance decoding logic supplies an output to selector switch driver logic 28 which selects various combinations of discrete capacitance from a capacitor array 30. These values are then added to the frequency determining resonant network of VCO 18. The output of capacitor array 30 may be one or any combination up to and including all of the capacitance. When added to the frequency determining circuit this achieves a course value of tuning for the frequency determining resonant circuit of VCO 18.

In operation, the frequency to capacitance decoding logic interprets from a predetermined value the appropriate capacitance which must be added to the VCO to enable the VCO to tune in a low power vernier manner to achieve the resultant frequency F_0 . The selector switch driver logic responds to the frequency to capacitance decoding logic to merely select and latch which capacitors in the capacitor array 30 must be coupled into the circuit to achieve the course tuning.

Thus, it may be seen that for various frequencies, rather than tuning the VCO with a high voltage varactor network and correspondingly

-5-

consuming the power required to maintain it and combining that with an appropriate divisor in programmable divider 20, the present low power frequency synthesizer augments the tuning capability
5 of the VCO circuit as it is driven by an outside voltage source with discrete capacitor values to alter the tuning. The normal phase locked loop in combination with the altered coarse tuning provides the appropriate programmable frequency control ratio
10 so that the synthesizer may provide the final output frequency F_0 in the appropriate range for desired operation. It will be clear to those skilled in the art that the switching in of the capacitor array requires considerably less power than the power
15 required to drive the frequency determining resonant circuit of a VCO and maintain it at a fixed voltage and frequency output position for considerable lengths of time. Thus, it may be seen that the entire operation of the frequency synthesizer occurs
20 with considerably less power consumed and may be operated with considerable lower voltages.

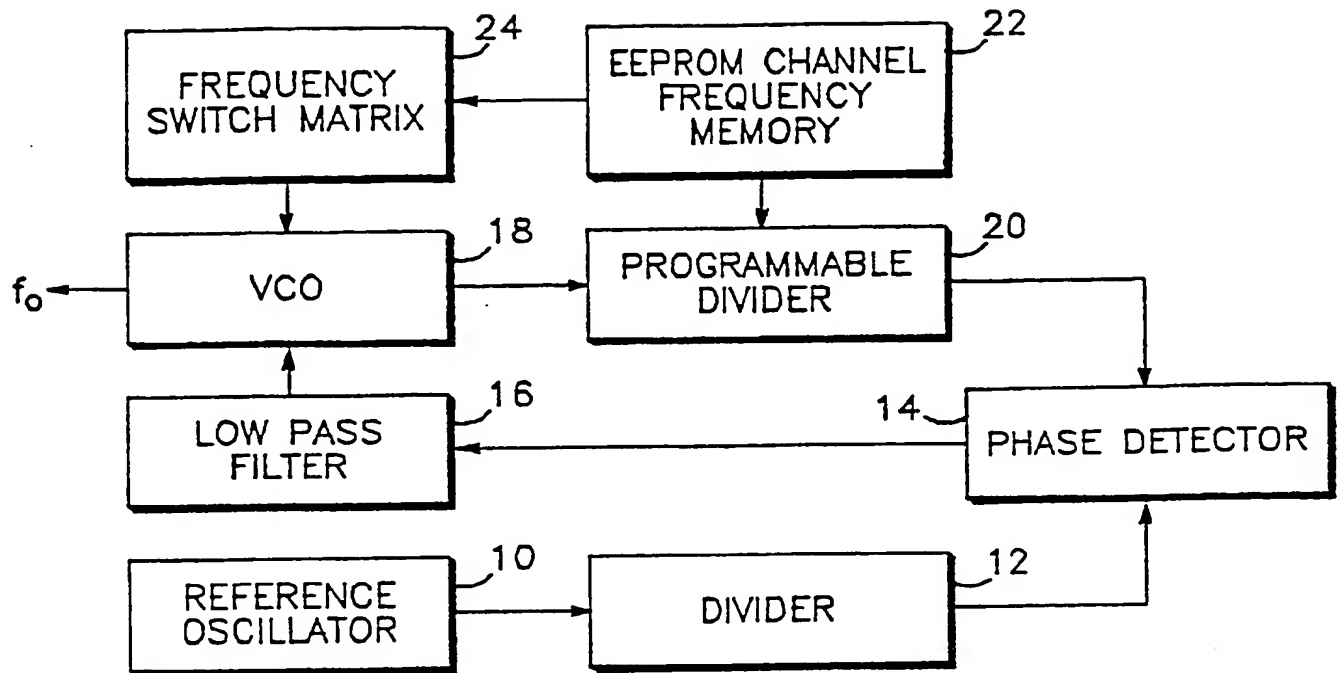
What is claimed is:

-6-

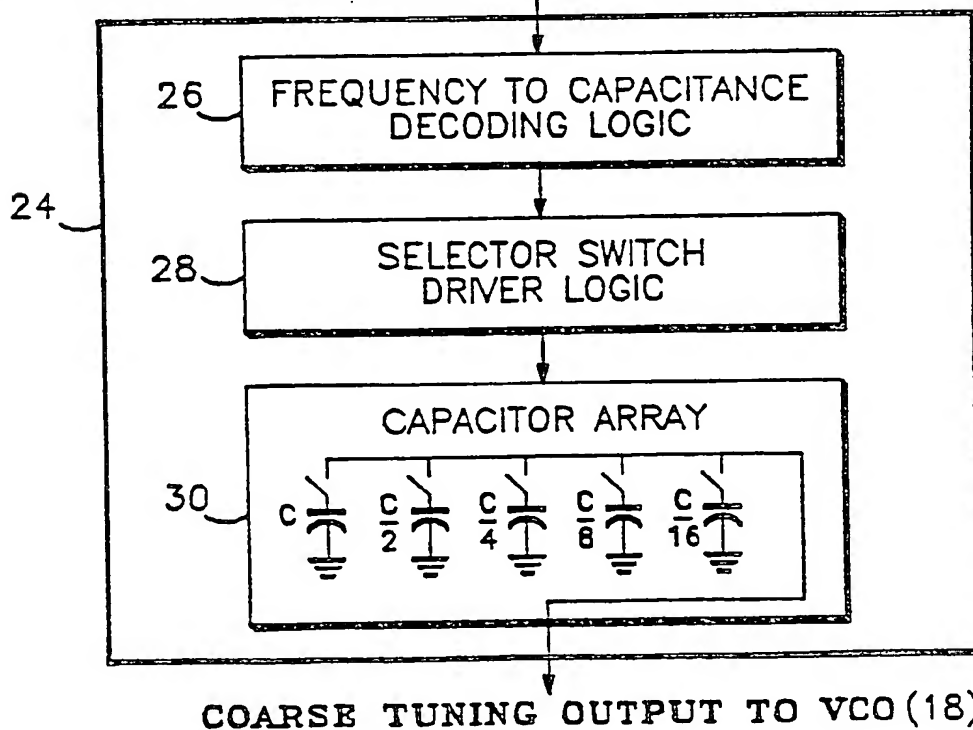
Claims

1. A low voltage and low power frequency synthesizer including a memory containing divisor information, a
5 variable divider phase locked loop responsive to the divisor information for controlling the output frequency of a voltage controlled oscillator comprising:
memory means (22) containing information
corresponding to the desired frequency and divisor
10 information of the VCO; and
frequency capacitance switch means (24) coupled
between said memory and said VCO responsive to additional
information to select a predetermined value of capacitance,
said switch means further including means producing a
15 coarse tuning frequency by augmenting the value of capacitance in the frequency determining network of the VCO, whereby a broad range of frequencies can be synthesized at lower voltages and maintained with lower
power consumption with the phase locked loop operating to
20 maintain the precision of the desired frequency.
2. The frequency synthesizer of claim 1, wherein the
memory means further comprises a programmable Read Only
Memory (ROM).
25
3. The frequency synthesizer of claim 2, wherein
said EROM is electrically erasable.
4. The frequency synthesizer of claim 1, further
30 including a plurality of capacitors (30) from which the frequency capacitance switch means may select.
5. The frequency synthesizer of claim 4, wherein the
plurality of capacitance (30) includes at least five values
35 in a binary related sequence.

1/1

FIG. 1**FIG. 2**

CHANNEL FREQUENCY DATA FROM EEPROM MEMORY (22)



INTERNATIONAL SEARCH REPORT

International Application No. PCT/US88/04547

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ⁶ According to International Patent Classification (IPC) or to both National Classification and IPC IPC (4): H03B 19/00; H03L 7/00 US CL: 307/271; 328/14,155; 331/1A																	
II. FIELDS SEARCHED <div style="text-align: center;">Minimum Documentation Searched ⁷</div> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 15%;">Classification System</th> <th style="width: 85%;">Classification Symbols</th> </tr> <tr> <td>US</td> <td>328/14,15,155 307/262,271 331/1A,16,17,18</td> </tr> </table> <div style="text-align: center;">Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸</div>			Classification System	Classification Symbols	US	328/14,15,155 307/262,271 331/1A,16,17,18											
Classification System	Classification Symbols																
US	328/14,15,155 307/262,271 331/1A,16,17,18																
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹ <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 10%;">Category [*]</th> <th style="width: 70%;">Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²</th> <th style="width: 20%;">Relevant to Claim No. ¹³</th> </tr> <tr> <td>A</td> <td>US, A, 4,613,826 (Masuko et al) 23 September 1986.</td> <td>1-5</td> </tr> <tr> <td>A</td> <td>US, A, 4,453,136 (Kelland) 05 June 1984.</td> <td>1-5</td> </tr> <tr> <td>A</td> <td>US, A, 4,330,758 (Swisher et al) 18 May 1982</td> <td>1-5</td> </tr> <tr> <td>A</td> <td>US, A, 4,305,045 (Metz et al) 08 December 1981</td> <td>1-5</td> </tr> </table> <div style="margin-top: 20px;"> Docket # <u>P2001, 0328</u> Applic. # _____ Applicant: <u>B. Balm et al.</u> <div style="text-align: center;"> Lerner and Greenberg, P.A. Post Office Box 2480 Hollywood, FL 33022-2480 Tel: (954) 925-1100 Fax: (954) 925-1101 </div> </div>			Category [*]	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³	A	US, A, 4,613,826 (Masuko et al) 23 September 1986.	1-5	A	US, A, 4,453,136 (Kelland) 05 June 1984.	1-5	A	US, A, 4,330,758 (Swisher et al) 18 May 1982	1-5	A	US, A, 4,305,045 (Metz et al) 08 December 1981	1-5
Category [*]	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³															
A	US, A, 4,613,826 (Masuko et al) 23 September 1986.	1-5															
A	US, A, 4,453,136 (Kelland) 05 June 1984.	1-5															
A	US, A, 4,330,758 (Swisher et al) 18 May 1982	1-5															
A	US, A, 4,305,045 (Metz et al) 08 December 1981	1-5															
<div style="display: flex; justify-content: space-between;"> <div style="width: 48%;"> <p>[*] Special categories of cited documents: ¹⁰</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 48%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"d" document member of the same patent family</p> </div> </div>																	
IV. CERTIFICATION <table style="width: 100%;"> <tr> <td style="width: 50%;">Date of the Actual Completion of the International Search</td> <td style="width: 50%;">Date of Mailing of this International Search Report</td> </tr> <tr> <td style="text-align: center;">28 March 1989</td> <td style="text-align: center;">04 MAY 1989</td> </tr> <tr> <td>International Searching Authority</td> <td>Signature of a Authorized Officer</td> </tr> <tr> <td style="text-align: center;">TSA/US</td> <td style="text-align: center;">Timothy P. Callahan</td> </tr> </table>			Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	28 March 1989	04 MAY 1989	International Searching Authority	Signature of a Authorized Officer	TSA/US	Timothy P. Callahan							
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report																
28 March 1989	04 MAY 1989																
International Searching Authority	Signature of a Authorized Officer																
TSA/US	Timothy P. Callahan																